ATS4000 Advanced Test System

Descriptions & Definitions of ADC Tests

as Implemented on the ATS4000

Version: D

Lynium

September 11, 2002
Tucson, Arizona

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Document:
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Version D
September 11, 2002
Lynium Document Number: ATS4K03D

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Abstract

This document describes and defines the basic analog-to-digital converter (ADC) tests that are implemented on the ATS4000 as of the date given. Both “DC” tests (offset error, gain error, integral non-linearity, and differential non-linearity) and “AC” tests (total harmonic distortion, signal-to-noise ratio, signal-to-(noise plus distortion), and spurious-free dynamic range) are covered. For each test, the basic test algorithm is described, pertinent equations given or described, and approximate test times presented.

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1. DC Testing Explained

The basic DC tests include offset error, gain error, differential nonlinearity (DNL), and integral nonlinearity (INL). An additional, implied test is for no missing codes (specified to a given resolution). This test is actually a different way of expressing differential nonlinearity.

The hardware requirements for the basic DC tests include a servo-loop circuit for the device under test (DUT) and a high-resolution digital voltmeter (or digital multi-meter [DMM]) with a minimum of 6½ digits of resolution, with 8½ digits preferred. The servo-loop circuit accepts a target code for the DUT (in this case, the ADC under test). It then servos the analog input voltage to the DUT (while it is converting) until the target code is seen at the ADC output.

There is one critical item regarding a servo loop system. The servo loop can force a voltage which produces the target code as a mean output value or the target code plus ½ as the mean output value. For example, if the target code is the mean value, then it will produce the target code exclusively or any output codes which are not the target code will be distributed evenly above and below the target code. If the target code + ½ is produced, then the target code will be produced as often as the code at target code plus one.

As an example, for 12-bit converters, it is important that the servo loop system use the later method (target code plus ½). This is not only the easiest to implement, but the first method suffers from uncertainty when the converter has very low internal noise. The reason is that there are a range of input voltages which will produce the target code exclusively for a low-noise 12-bit converter. For the target code plus ½ method, the input voltage that produces this situation has a very small range, far below the "voltage" size of a single LSB. This method is sometimes referred to as finding the code "edge" (or code transition).

For all the DC tests, Web Technologies uses a servo loop system that servos to the target code plus ½ (the servo loop will settle to a voltage where the converter's output code varies evenly between J and J+1). This item will be critical for proper correlation to other test equipment.

Also note that the distribution of output codes for code J or lower is equal to the number of output codes at J+1 or higher. If code J or J+1 is missing, the proper voltage will still be produced unless code J is 0 or code J+1 is 2^N–1 (where N is the resolution, in bits, of the analog-to-digital converter). If either of the two end codes is missing, then the servo loop will produce the wrong voltage.

In addition to the servo loop circuit and DMM, a computer is required to control the target code and to read the result from the DMM. Computer software will then be able to determine offset error, gain error, INL, and DNL. From the DNL results, the no-missing-code status of the DUT can be determined.

Regarding INL testing, there are two methods to compute INL: the "end-point" method and the "best-fit" method. The end-point method relates the INL to a straight line drawn through the end-points of the converter's transfer function. The best-fit method relates the INL to a straight line which best fits the transfer function. (Note that the end-point method can produce results up to two times greater [worse] than the best-fit method, but the best-fit method can never produce numbers worse than the end-point method. In other words, the endpoint method is the most conservative way to measure the ADC's linearity. Thus, the end-point method is also considered a more "honest" measurement.)

2. Definitions of DC Test Parameters (measured with a servo-loop setup):

For simplicity, the following discussion assumes an analog-to-digital converter with a unipolar input range of 0V to V_{REF} (internal or external reference voltage). Some ADCs offer a bipolar input range of $-V_{REF}$ to $+V_{REF}$ or may provide a scaling factor which divides the analog input voltage by some value. So, the actual input range might be from 0V to SF • V_{REF}, –(SF • V_{REF}) to +(SF • V_{REF}), or even –(SF • V_{REF} + OF) to +(SF • V_{REF} + OF) where SF is a scaling factor and OF is an offset factor.

Rather than complicate the discussion with the many different possibilities, the definitions of the DC parameters assume an ADC whose input range is 0V to V_{REF}. If the actual ADC input is scaled but is still unipolar, the modifications to the equations are trivial. If the input range is bipolar, then the changes are slightly more complicated, but still derive from the basic equation presented here. (The biggest difference for a bipolar ADC is the possibility of defining both a positive gain error and a negative gain error.)

In the discussion that follows, numbers with a lower case H at the end are in base 16 (hexadecimal) format; N is the resolution of the converter (in bits); V_{ZS} is the voltage which produces the transition between the zero-scale code and the next highest code (12-bit ADC example: 000_H and 001_H); V_{FS-1} is the voltage which produces the transition between the full-scale code minus one and the full-scale code (12-bit ADC example: FFE_H and FFF_H); $V_{J:J+1}$is the voltage which produces the transition between code J and code J+1 ($V_{0:1} = V_{ZS}$ and, for a 12-bit converter, $V_{FFE:FFF} = V_{FS-1}$); and ILSB is the voltage "weight" of an ideal least significant bit, as defined by:

$$\text{ILSB (in volts)} = V_{REF}/2^N.$$

In regards to the provided test times, note that the range would not cover the initial test setup. The reason for this is that, in most cases, measurements are made along with other measurements and the setup time must be factored among them. It typically requires one to three seconds to properly configure the ATS4000 in order to begin testing and approximately one second to turn everything off once testing is complete. If the DUT is to be tested over temperature, the test setup will only happen once at the beginning of testing and shutdown will only occur at the end (when the next DUT is to be installed).

Also, the test times that are given assume a conversion rate of 100kHz or faster. If the ADC is slower than 100kHz, test times will increase (the servo loop method requires at

least 1000 conversions in order to achieve good results and repeatability). It is difficult to measure DC parameters when the conversion rate is lower than 10kHz and the lower limit is generally around 1kHz. At that point, test times will have increased dramatically (one second or longer to measure each transition voltage). Methods other than the servo loop are recommended for low conversion rates, but these will not substantially increase test times.

2.1. **Offset Error**: V_{ZS} is measured. From this voltage reading, ½ of an ideal least significant bit (LSB) "weight" is subtracted, producing the value of the zero-scale voltage. This is also the offset error voltage. If expressed in LSBs, the offset error voltage is divided by the weight of an average LSB.

$$\text{Offset Error (in LSBs)} = (V_{ZS} - 0.5 \bullet \text{ILSB}) / \text{ILSB}$$

Test time: A typical test time would be 10ms to 100ms, depending on the resolution of the ADC.

2.2. **Gain Error**: V_{FS-1} is measured. The voltage of the reference is also measured. From the reference voltage, 2 ideal LSB weights are subtracted, producing an ideal value which represents the input span of the converter from the zero-scale transition to the full-scale minus one transition. The actual zero-scale transition voltage is measured (if not already measured) and subtracted from the measured full-scale transition voltage. The resulting value is subtracted from the ideal voltage span of the converter. If expressed in LSBs, the gain error voltage is divided by the weight of an ideal LSB.

$$\text{Gain Error (in LSBs)} = (V_{REF} - 2 \bullet \text{ILSB} - (V_{FS-1} - V_{ZS})) / \text{ILSB}$$

Test time: A typical test time would be 10ms to 100ms, depending on the resolution of the ADC.

2.3. **Integral Nonlinearity (INL)**: The target code is initially set to zero-scale and the V_{ZS} voltage measured. Then the V_{FS-1} voltage is measured. If these two values are reasonable, then INL testing continues. (The case of a missing code at full-scale is not handled with this test algorithm. The servo-loop will "rail" if the full-scale code is missing and the voltage will be much greater than it would normally be, so testing will stop.) The target code is then swept from zero-scale to full-scale. When each code transition has settled, the input voltage is measured. The integral nonlinearity at that code is:

$$\text{INL}_J \text{ (in LSBs)} = (V_{J:J+1} - (J \bullet \text{ALSB} + V_{ZS})) / \text{ALSB}$$

Where J is the target code, $V_{J:J+1}$ is the measured transition voltage between code J and J+1, and ALSB is the actual voltage weight of each LSB as computed by the following equation:

$$\text{ALSB (in volts)} = (V_{FS-1} - V_{ZS}) / (2^N - 2)$$

Note that offset and gain error could use ALSB for expressing their respective errors in LSBs or INL could use ILSB for expressing its error in LSBs. However, the specifications for most ADCs imply that gain and offset error are relative to an ideal LSB while INL and DNL are relative to an actual LSB (note that this is open to some debate). In reality, the difference between ALSB and ILSB is usually extremely small. Again, the key point of this document is to provide a definition that can be used for correlation purposes.

The definition that has just been provided for INL relates the value of each individual code to the endpoint transitions and is referred to as the endpoint method (compared to the "best-fit" method). Also, the INL for the zero-scale code and the full-scale minus one LSB code is, by definition, zero. The INL for the full-scale code cannot be measured.

Due to temperature drift, the endpoints may be re-measured periodically during an all-codes test if test times are excessive. Each setup should be tested to determine how it drifts with time in order to calculate how often endpoints should be re-measured. If the test in progress exceeds the maximum allowable time, the endpoints (zero-scale and full-scale minus one LSB) will be re-measured and these voltages become the new V_{FS-1} and V_{ZS}. (Note that because of this, INL must be calculated as the test is performed. The measured voltages cannot simply be stored in an array and INL calculated at the end of the test.)

Test time: A typical INL measurement requires 10ms to 100ms per code, depending on the resolution of the ADC. Thus, an all-codes INL test would require $2^N/100$ to $2^N/10$ seconds (actual 12-bit ADC test times: 60 seconds to 5 minutes). Note that it is possible to measure only certain output codes rather than all output codes, provided that the codes are selected carefully. This can reduce the test time by one to three orders of magnitude.

2.4. **Differential Nonlinearity (DNL)**: The target code is initially set to zero-scale and the V_{ZS} voltage measured. Then the V_{FS-1} voltage is measured. If these two values are reasonable, then DNL testing continues. (The case of a missing code at full-scale is not handled with this test algorithm. The servo-loop will "rail" if the full-scale code is missing and the voltage will be much greater than it normally would be, so testing will stop.) For all-code DNL testing, the target code is then swept from zero-scale to full-scale minus one LSB. When each code transition has settled, the input voltage is measured. The differential nonlinearity at that code is:

$$DNL_J = (V_{J:J+1} - V_{J-1:J}) / ALSB - 1$$

Where J is the target code, $V_{J:J+1}$ is the measured transition voltage between code J and J+1, $V_{J-1:J}$ is the measured transition voltage between code J–1 and J, and ALSB is the actual voltage weight of each LSB as computed by the following equation:

$$ALSB \text{ (in volts)} = (V_{FS-1} - V_{ZS}) / (2^N - 2)$$

See the INL discussion for comments regarding ILSB vs. ALSB. Note that DNL is computed in the same manner regardless of which INL method is used (endpoint or "best-fit"). For DNL testing, it is not necessary to re-measure the endpoints during the test. However, INL and DNL are usually calculated at the same time, so the endpoints may be re-measured to produce more accurate INL results.

Test time: A typical DNL measurement requires 10ms to 100ms per code, depending on the resolution of the ADC. Thus, an all-codes DNL test would require $2^N/100$ to $2^N/10$ seconds (actual 12-bit ADC test times: 60 seconds to 5 minutes). Note that it is possible to measure only certain output codes rather than all output codes, provided that the codes are selected carefully. This can reduce the test time by one to three orders of magnitude.

3. DC Test Example

Figure 1 shows an example of the DC test results for a 12-bit, 100kHz ADC. Note that this converter has three missing codes.

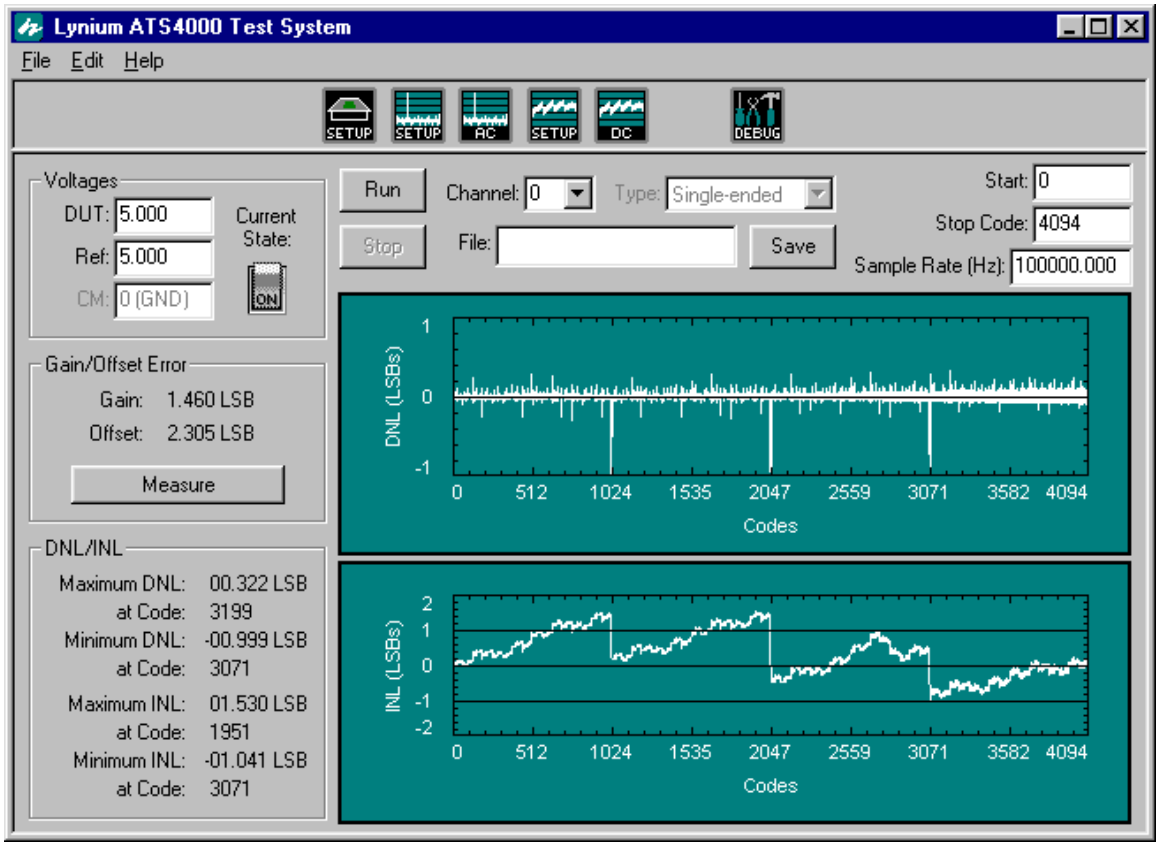

Figure 1. DC Test Results for a 12-bit, 100kHz ADC.

4. AC Testing Explained

The basic AC tests include total harmonic distortion (THD), signal-to-(noise plus distortion) ratio (SINAD), signal-to-noise ratio (SNR), and spurious-free dynamic range (SFDR). Note that an additional AC test is inter-modulation distortion (IMD), which is not covered in this document.

The hardware requirements for basic AC testing include a method of generating a very pure sinewave of the required amplitude and offset, a clock generator that can be locked to the sinewave generator, a method to capture continuous data (at least 4096 points) from the device under test (DUT), and computer to process the data with a fast Fourier transform (FFT) algorithm. Calculations on the FFT result yield THD, SNR, SINAD, and SFDR.

A critical item regarding AC testing is the need for the clock generator and the sinewave source to be "locked" together. This means that each generator uses the same reference frequency. In addition, each generator must be programmable to a high enough resolution in order for the two generators to track each other over the time frame of the data acquisition period to a level below that of the ADC's resolution. This usually requires that the generators be programmable to a millihertz resolution (the requirement is dependent on the resolution and performance of the converter). This AC test method is known as "coherent" testing and eliminates the need for a window function (such as a four-term Blackman-Harris window, Hanning window, etc.).

Coherent testing also means that the input signal contains an exact number of cycles over the data acquisition period. For proper coherent testing, the number of cycles should be an odd number. This reduces the chance that a harmonic of the fundamental will occur at the exact location of the fundamental, another harmonic, or the DC bin. A stricter requirement is that the number of cycles be a prime number.

The software requirements include the ability to program the clock generator and sinewave source. AC testing usually requires that the computer directly control the frequency of both generators because it may not be possible to set the generators to a high enough resolution from their respective front panels. The software must also be able to obtain the captured data, to process the data with an FFT, to perform the necessary calculations, and to output the results.

The repeatability of the AC tests is dependent on the test being performed, the performance of the converter, and the number of points in the FFT. The larger the number of points in the FFT, the more repeatable the numbers. However, test time goes up with the number of points in the FFT.

Note that when the harmonics and spurs in the FFT result are on the order of the noise floor of the FFT, the repeatability of some AC measurements will go down. This typically affects THD and SFDR when the converter has a good sample-and-hold, a very linear transfer function, and when the results are expressed in decibels. For THD and

SFDR, it is sometimes better to express the results in absolute power as there in no effective solution to obtaining better repeatability with results expressed in decibels.

5. Definitions of AC Test Parameters (all performed with the AC test setup):

Usually, very little time is required to obtain the AC test results. However, it can be longer if the conversion rate of the ADC is very low. Assuming that the converter is 100kHz or higher, 4096 data points can be collected in 41ms. The computer then computes the FFT and derives the AC parameters from the resulting data. This generally takes 100ms or less for a Pentium II class computer (or faster).

Including time to display the results (or save them to a file), all of the following AC parameters can be measured within 300ms. This time does not include setup time. It typically requires one to three seconds to properly configure the ATS4000 in order to begin testing and approximately one second to turn everything off once testing is complete. Test setup and shutdown may occur only once when the DUT is installed and removed, so this overhead may be minimal.

If the conversion rate of the ADC is low (slower than 100kHz), then the time required to collect 4096 data points can become excessive (for example, 4.096 seconds for a 1kHz conversion rate). Test time can be reduced by using a lower number of points for the FFT, but there are trade-offs relative to DUT performance and measurement repeatability.

5.1. **Total Harmonic Distortion (THD)**: The power of M harmonics of the input frequency (known as the fundamental) are summed. THD is the power in the harmonics divided by the power in the fundamental and is expressed in dBc (20 times log of the ratio, dBc stands for dB relative to the carrier). The harmonics must not lie at the DC bin (leftmost bin of the FFT), the fundamental, or any other harmonic. Requiring that the number of cycles of the input signal digitized during the data acquisition period be an odd number is usually sufficient to meet this requirement. However, this is not always the case, and a prime number is recommended.

The number of harmonics, M, is usually in the range of five to nine, but there are cases where it is beneficial to use a lower or higher number. The default number that is used by Lynium is five. However, the software will accommodate any number of harmonics up to 99.

Note that the harmonics must be accounted for carefully if their frequency is greater than Nyquist (½ the conversion rate). Any harmonic whose frequency is greater than the Nyquist frequency will alias to a new position in the FFT result. Harmonics whose frequencies are greater than the conversion rate are computed based on the remainder of the harmonic frequency modulo the conversion rate. All such aliasing is handled automatically by the ATS4000 software.

5.2. **Signal-to-(Noise and Distortion) Ratio (SINAD)**: The sum of all the power in the FFT result except for the fundamental bin and the DC bin is computed. SINAD is the ratio of the power in the fundamental to this total power and is expressed in dB (20 times the log of the ratio).

5.3. **Signal-to-Noise Ratio (SNR)**: The sum of all the power in the FFT result is computed with the exception of the following: the fundamental bin, the DC bin, and the M harmonic bins used in the THD calculation. SNR is the ratio of the power in the fundamental to this total power and is expressed in dB (20 times the log of the ratio).

5.4. **Spurious-Free Dynamic Range (SFDR)**: The FFT result is searched for the highest spur which is not the DC bin or the fundamental bin. The power of the spur is subtracted from the fundamental power and the result expressed in dBc (20 times the log of the difference, dBc stands for dB relative to the carrier).

The highest spur is generally, but not always, the second harmonic. In some definitions of SFDR, the search for the highest spur excludes the M harmonic bins which are used for the THD calculation. In other definitions, the search for the highest spur includes only the harmonic bins. There are specific reasons why this is done for certain types of converters. However, for SAR converters, the search is generally performed over the entire FFT result. The ATS4000 uses the later method to find the highest spur.

6. AC Test Example

Figure 2 shows an example of the AC test results for a 12-bit, 100kHz ADC. Note that this converter has extremely good linearity—the harmonics of the fundamental are not visible above the noise floor. This converter is not the same device whose DC results are shown in Figure 1.

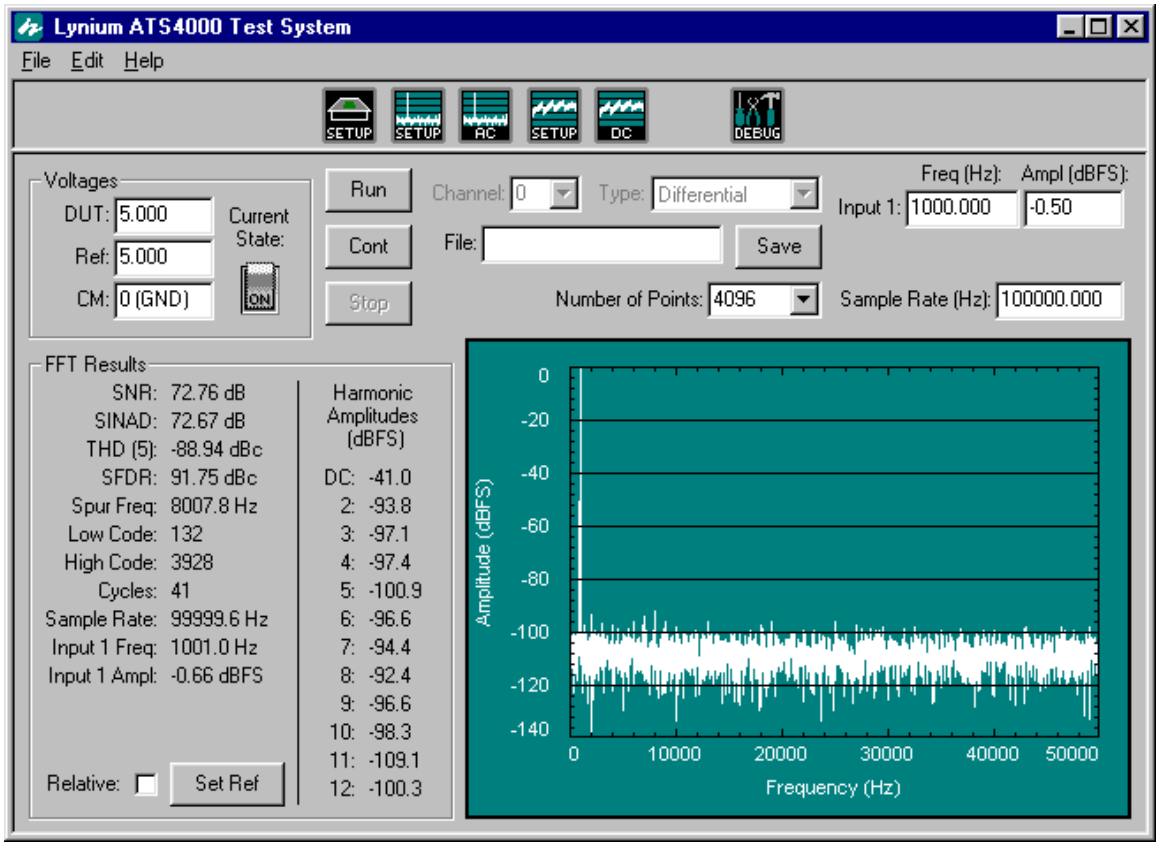

Figure 2. AC Test Results for a 12-bit, 100kHz ADC.

Revision History

Rev.	Date	Comment
A	March 21, 2000	Initial Release
B	March 23, 2000	Added copyright notice on all pages and figures 1 and 2
C	May 18, 2000	Revised figures 1 and 2
D	September 11, 2002	Revised text in section 2.2

