ATS4000 Advanced Test System

The ATS4000

A Flexible Test System for Mixed-Signal Components

Version C

Lynium

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The ATS4000: A Flexible Test System for Mixed-Signal Components
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Author:
Jerry Horn
Senior Design Engineer
Lynium LLC
2030 N Forbes Blvd, Suite 102
Tucson, AZ 85745
Phone: (520) 579-0047
Fax: (520) 579-8712
E-mail: jhorn@lynium.com

Company:
Lynium LLC
2030 N Forbes Blvd, Suite 102
Tucson, AZ 85745
Phone: (520) 579-0047
Fax: (520) 579-8712
Web site: www.lynium.com

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Abstract

This document discusses the problems inherent in testing high-performance mixed integrated circuits or circuit modules which are part of a larger integrated circuit. Systems and procedures for accomplishing the task are described. One proposed solution, the ATS4000, is compared and contrasted to other solutions including the use of production test equipment and "ad-hoc" test fixtures.

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1. Introduction

Engineering evaluation, device characterization, and production monitoring of the performance of mixed-signal components is both a simple and complex task. Aspects of the testing process are fairly straightforward. However, for high-performance mixed-signal devices, the test platform must provide even higher performance test signals and very precise measurement equipment. In addition, the device under test (DUT) must tested over a wide variety of configurations. Add to this the increasing digital complexity of many mixed-signal devices, and what should be a simple test procedure quickly becomes a very difficult task.

Rather than continue to look at the task in abstract terms, here is a specific example. Assume the goal is to test an 8-channel, 12-bit, 100 kHz analog-to-digital converter (ADC). The specifications for an ADC include the following:

Specification	Test setup must provide the following answer
Offset Error	What input voltage produces the code 0 to 1 transition?
Gain Error	What input voltage produces code 4094/4095 transition?
Integral Non-Linearity (INL)	How does the ADC’s transfer function deviate from a straight line?
Differential Non-Linearity (DNL)	How does the ADC’s code width vary from code-to-code?
Signal-to-Noise Ratio (SNR)	How much noise is added to an ideal input signal?
Total Harmonic Distortion (THD)	How much distortion is added to an ideal input signal?

For a 12-bit ADC, the task of measuring offset error, gain error, INL, and DNL typically falls to a high-performance voltmeter such as an HP 3458A from Agilent Technologies. This digital multimeter provides up to 8½ digits of resolution, allowing for repeatable voltage measurements down to the microvolt level.

This level of performance is more than is needed for a 12-bit ADC whose guaranteed offset error will typically be two or three millivolts. However, the goal is to be able to measure the offset error at least ten times better than the guaranteed specification. This means repeatable measurements below 100 microvolts.

In addition, modern 12-bit ADCs can be operated from voltages as low as 2.0 V and may have an input voltage range which is similar. The least significant bit weight (abbreviated LSB) of the ADC could be as low as 2.0V/4096 or 488µV. Measurements for offset error, gain error, INL, and DNL must all be at least ten times better than the LSB size—in this case, repeatable to less than 50µV.

While the HP 3458A may still offer higher performance than is needed, it is generally a “safe bet.” The cost of the unit (approximately $8,000) is low when compared to the engineering effort required for characterization and validation, particularly when this cost is spread over a large number of devices.

Likewise, measuring SNR and THD generally requires a very high performance sine wave generator which is at least ten times better than the ADC. A 12-bit device requires a generator whose SNR and THD are greater than 85 dB. The ADC will also be tested over various frequencies, so it is a good idea to have a generator than can hold this specification or better beyond 20 kHz. The generator must also be very stable, offer high frequency resolution (millihertz frequency resolution or lower), and must either provide a reference clock or be lockable to an external reference clock.

As with the voltmeter, such generators are not low cost. The best generator for the task is approximately $15,000. In the case of high-speed ADCs (conversion rates of several megahertz and beyond), even higher performance and higher cost generators are necessary. However, the point is the not the cost of the unit, but the fact that it must meet a certain level of performance and than level is very high for even a low-speed, 12-bit ADC.

2. Production Test Equipment

Standard production test equipment from companies such as Eagle, LTX, and Teradyne provide solid solutions for testing a wide variety of digital products. In addition, some low performance mixed-signal devices can be tested as well. The main problem lies with the testing of either stand-alone, high-performance mixed-signal devices or high performance mixed-signal devices which have been embedded within a large digital integrated circuit (IC).

In many cases, equipment such as the HP 3458A and high-quality sine generators must be added to the testers in order to accomplish the production testing. In a few cases, the manufacturer may be able to add a module to the tester that provides limited but adequate performance. Such modules are usually very specific to the test requirements, may require a number of months to develop, and will not be low cost.

Production testing of a high-performance mixed-signal device on standard production test equipment is currently a matter of creating a “good enough” solution. Even after adding a meter such as the HP 3458A, low level voltage measurements may not be repeatable. This is generally due to the presence of high-speed digital signals in the test head fixture, long cable lengths, contact resistance of pogo pins, and the EMI/RFI interference from handlers, temperature forcing units, and miscellaneous electronic equipment.

Thus, high-performance mixed-signal devices must be characterized in the laboratory first. Because time is limited, this characterization system must be flexible without compromising performance. Once the device has been fully characterized, the test engineer can target the test solution towards providing the required level of performance. In addition, the tests that are implemented can be chosen with the confidence that they will provide adequate test coverage and ensure that the device meets all of its guaranteed specifications.

3. Bench-top Characterization and Validation

In the past, there have been no general purpose “bench-top” characterization systems aimed at the high-performance mixed-signal market. Apparently, each manufacturer of mixed-signal components has solved the problem in a different way or may simply solve the problem for each individual component.

For example, small test boards and custom programs might be created to test the component’s key specifications. Each test board would be specific to the unit and, once characterization was complete, the board would be passed over to production or locked away in a cabinet. In many cases, the board quickly becomes of little use due to lack of documentation and/or lost software. (It should be noted that there are a few tests where creating a custom board is the only solution to achieving a test result in a reasonable period of time.)

Because of the limited abilities of the custom test solution (both hardware and software), the design engineer may not be able to completely characterize certain parameters or test certain configurations of the device. If some parameters are not fully characterized, two problems will result: either the parameters will not be guaranteed in the datasheet or the specifications will be reduced. In some cases, it might be decided that certain parameters should not be guaranteed or specifications lessened. However, this is a decision that should be made because of marketing concerns and not simply due to lack of data.

In addition, if the device cannot be tested in certain configurations, then the design engineer may be forced to assume that the performance will be reasonable or will attempt to infer the performance from other test configurations which are similar. In each case, there is a risk that the performance of the device might be lower than expected. Such a situation can be disastrous if the end-user is the one who first learns of the poor performance. In addition, lack of performance data can reduce the quality of the datasheet and the recommendations that can be included in regards to getting the best performance.

4. The ATS4000

The ATS4000 attempts to strike a balance between an “ad-hoc” custom bench-top characterization setup and a production tester. A typical setup is shown in Figure 1.

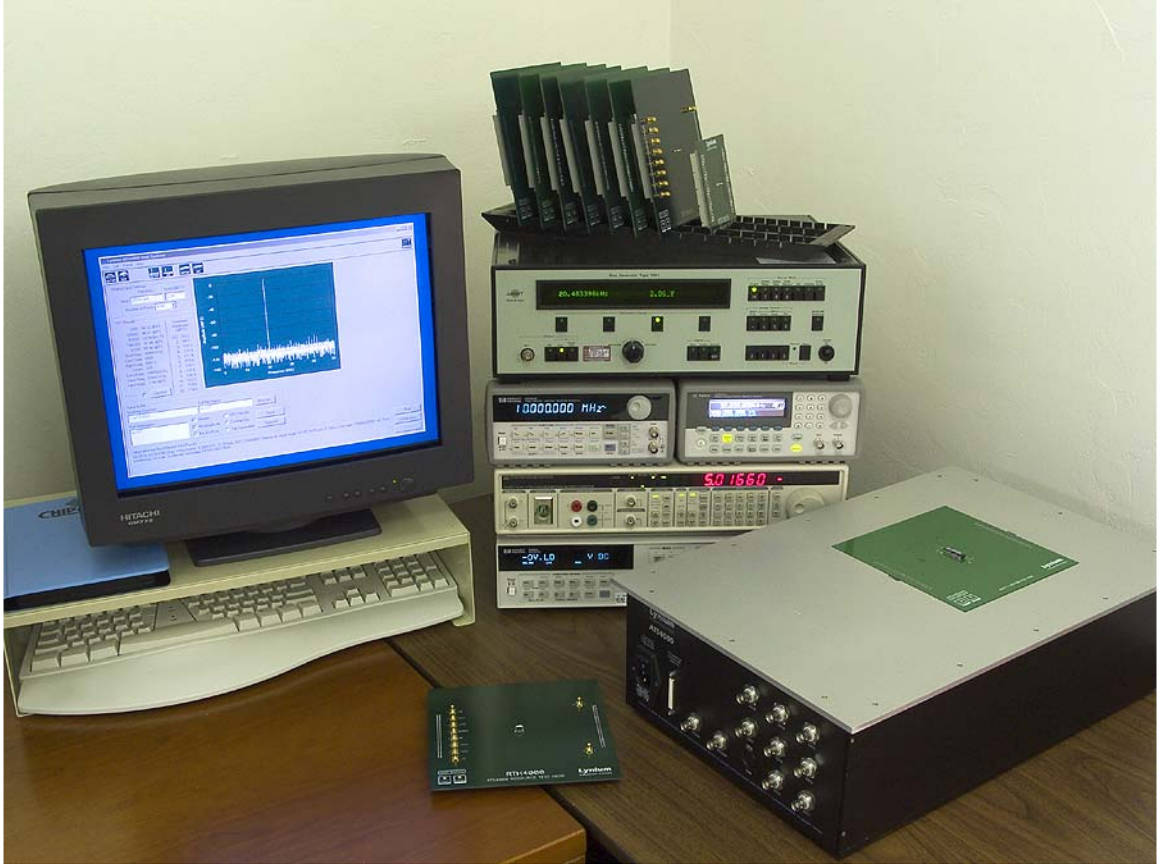


Figure 1. Typical ATS4000 Setup

The ATS4000 has been used to test the following types of ADCs and digital-to-analog converters (DACs):

- 10-bit, 15 MHz, pipelined ADC
- 12-bit, single-ended, 100 kHz, successive-approximation-register (SAR) ADC
- 13-bit, fully differential, 100 kHz, SAR ADC
- 16-bit, fully differential, 1 MHz SAR ADC
- 24-bit, 7.5 Hz delta-sigma ADC
- 10-bit, 50 MHz DAC
- 16-bit, 50 MHz DAC
- A variety of 12-bit and 16-bit industrial DACs

In order to provide this flexibility, the ATS4000 offers the following features:

- Main ATS4000 unit. The ATS4000 system offers basic functionality: power supplies of ±5V and ±15V; low-noise programmable power supplies (5µVrms or less); high-speed, low noise 16-bit DACs for flexible generation of ‘DC’ voltages (5µVrms or less); uncommitted digital I/O lines connected to a programmable logic device; and uncommitted analog inputs and outputs which are available at the unit’s side panel.

Figure 2. ATS4000 Side View.

- Extensible resources via a variety of daughtercards. Various daughtercards can be used with a test head in order to provide additional resources that are not included in the ATS4000 itself. These daughtercards provide high-speed (80 MHz) digital pattern generators, high-speed (50 MHz) data collectors, high-precision voltage sources, and very high stability voltages sources.

Figure 1. ARM5606 Daughtercard Provides Six High-Resolution, High-Stability DC + AC Voltage Sources.

- Automatic test head detection. Each test head has a unique identification code which is read by the PC software. This code is used to determine which files must be downloaded to the ATS4000 system and to configure the PC software for the appropriate tests. This process is completely automatic.

- Minimal test head jumpers. Many stand-alone characterization boards have a large number of jumpers to configure the DUT in various ways. The goal of the ATS4000 has been to eliminate all test related jumpers on the test head. Some test heads do have a few jumpers, but these have been included only for device selection (if the test head supports multiple devices) or for experimentation purposes. In all cases, it is possible to make dedicated test heads with no jumpers. The elimination of all jumpers and self-configuring software means substantially fewer headaches in documentation, and eases the transition of test boards between design and production.

- Version control. All microcontrollers in the motherboard and the test head, each DSP program, every FPGA bit file, the main PC software, and all custom PC software components (DLLs) provide version control information. In addition, each ATS4000 contains a unique serial number. All of this information is included in the header every time data is saved and also appears on each test results display (in case a screen shot of the test results are saved).

- Each program version is “stand-alone.” The PC software is revised in a manner which allows new versions to be installed without “breaking” old versions. Any previous version can be executed at any time, if needed. (However, multiple versions of the PC software cannot be running at the same time.)

- Connection to external equipment: 1) An HP 3458A is used to read all DC voltages including programmable power supplies and analog inputs [this removes the need for calibrating these sources]; 2) Sine generator or generators; 3) External clock source; 4) Other external equipment as needed.

- Two paths for ADC testing: custom test heads designed by Lynium and supported by custom ATS4000 software or end-user developed daughtercards that work with the General Access Platform (GAP) 1616 and standard ATS4000 software (contact Lynium for more information regarding the GAP1616).

- The ATS4000 is not a production test system. However, it is designed to be used along side production test equipment: as a resource for analyzing poor yields or as a check for parameters that are sample tested only.

The ATS4000 provides a stable and capable platform for engineering evaluation and characterization. Such a system can offer big dividends: ever increasing software capability, ease-of-use, more complete characterization, simpler transition between design and production, better information for the datasheet, and more effective debug of new silicon. All of these add up to quicker time-to-market.

5. ATS4000 Features

The ATS4000 consist of three parts: the base system, the test head, and the software. Some test heads may also require a daughtercard. External test equipment is required, but the type and quantity of test equipment will vary depending on the testing to be performed.

The base system connects internal and external resources to a test head that plugs into it. External resources connect to the base unit through BNC connectors and a differential XLR connector. The XLR connector is used for DC measurements using a external DC voltmeter such as the HP3458 8½ Digit voltmeter. There are up to eight separate BNC connectors. These connect to the test head and internal motherboard using RG316 cable and MCX and SMA connectors. Trigger (output) and Clock (input) BNC connectors are also provided. Both connectors are compatible with TTL levels.

Internal resources consist of low-noise programmable power supplies, regulated fixed power supplies, high-speed pin drivers, digital I/O (FPGA), analog servo-loop, digital servo-loop, and a programmable voltage reference.

A PC interfaces to the ATS4000 using the parallel port (IEEE-1284 compatible). External instrument control is through an IEEE-488 bus.

Some test heads may also require a daughtercard that is attached to the bottom of the test head. There are currently two daughtercards that are supported by the ATS4000 software: the ARM6444 and the ARM5606. The ARM6444 provides a 80 MHz, 16-bit pattern generator; a 50 MHz, 16-bit data collector; 8 voltage sources; and 8 relay drivers. The ARM5606 supplies six high-resolution, high-stability, “DC+AC” voltage sources with a frequency range of 10 kHz and a frequency resolution of 2 pHz.

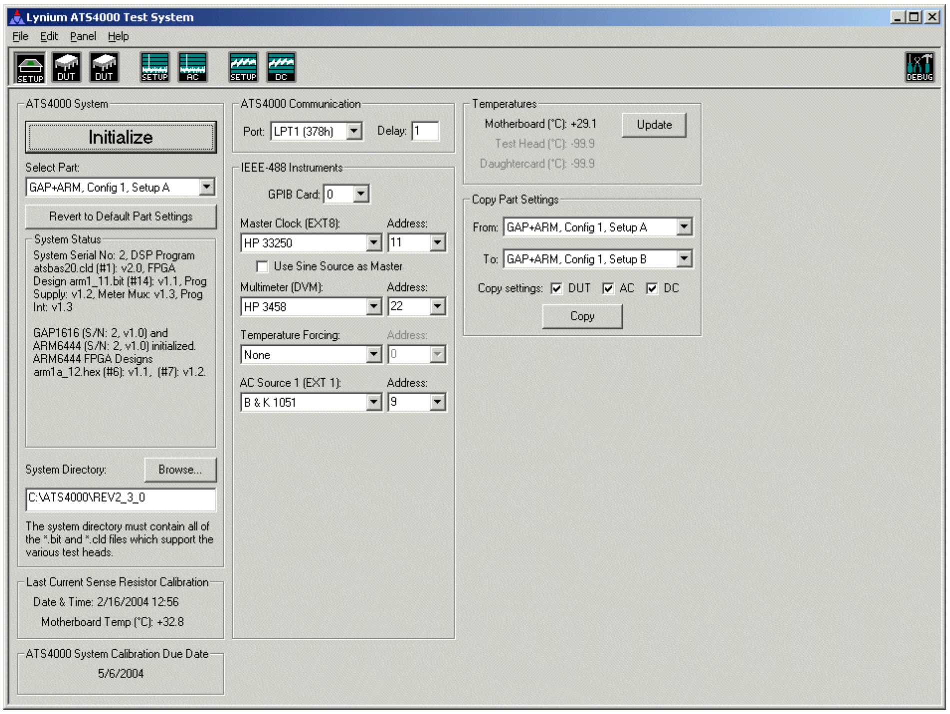
The test head accommodates a 6” diameter Thermostream™ temperature forcing chamber and all test heads include an identification code and serial number.

6. ATS4000 Software

The ATS4000 software is Windows 98, ME, 2000, and XP compatible. There are three primary tests supported:

AC Performance: SNR, SINAD, ENOB, THD, and SFDR
DC Linearity: Offset Error, Gain Error, INL, and DNL
Transfer Linearity: Offset Error, Gain Error, INL, and Output Noise

The ATS4000 software provides a modal structure where different test modes are selected via a series of icons on the test bar; which is located at the top of each ATS4000 panel. When the software is first started, the initial panel is the System Setup Panel, shown in Figure 4. This user interface provides the ability to initialize the ATS4000, monitor system status, and configure the external GPIB instruments.



ATS4000 System
Select Part: GAP+ARM, Config 1, Setup A

System Status
System Serial No: 2, DSP Program atsbas20.cld (#1): v2.0, FPGA Design arm1_11.bit (#14): v1.1, Prog Supply: v1.2, Meter Mux: v1.3, Prog Int: v1.3

GAP1616 (S/N: 2, v1.0) and ARM6444 (S/N: 2, v1.0) initialized. ARM6444 FPGA Designs arm1a_12.hex (#6): v1.1, (#7): v1.2.

System Directory: C:\ATS4000\REV2_3_0

The system directory must contain all of the *.bit and *.cld files which support the various test heads.

Last Current Sense Resistor Calibration
Date & Time: 2/16/2004 12:56
Motherboard Temp (°C): +32.8

ATS4000 System Calibration Due Date
5/6/2004

ATS4000 Communication
Port: LPT1 (378h)
Delay: 1

IEEE-488 Instruments
GPIB Card: 0
Master Clock (EXT8): HP 33250 Address: 11
☐ Use Sine Source as Master
Multimeter (DVM): HP 3458 Address: 22
Temperature Forcing: None Address: 0
AC Source 1 (EXT 1): B & K 1051 Address: 9

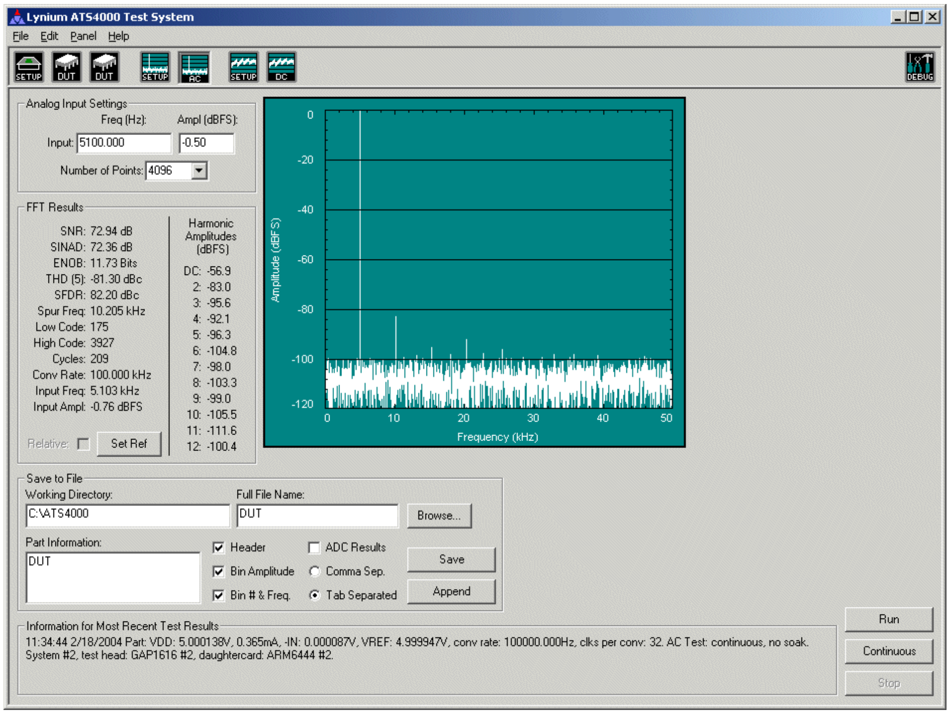
Temperatures
Motherboard (°C): +29.1
Test Head (°C): -99.9
Daughtercard (°C): -99.9

Copy Part Settings
From: GAP+ARM, Config 1, Setup A
To: GAP+ARM, Config 1, Setup B
Copy settings: ☑ DUT ☑ AC ☑ DC

Figure 4. Main System Panel (GAP1616 Test Head installed).

The first of the three tests to be described is the AC performance test. An example result for a 12-bit, 100 kHz ADC is shown in Figure 5. This test provides signal-to-noise ratio (SNR), signal-to-(noise plus distortion) (SINAD), equivalent number of bits (ENOB), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). A number of additional parameters are provided for help in interpreting the test results.

It is possible to run a single AC test or to perform continuous AC tests until the process is stopped by the user. For continuous testing, the display update rate is roughly two to three times per second (4k point FFTs), which provides a "real-time" feel for test optimization, troubleshooting, and debug.



Analog Input Settings

	Freq (Hz):	Ampl (dBFS):
Input:	5100.000	-0.50

Number of Points: 4096

FFT Results

SNR: 72.94 dB
SINAD: 72.36 dB
ENOB: 11.73 Bits
THD (5): -81.30 dBc
SFDR: 82.20 dBc
Spur Freq: 10.205 kHz
Low Code: 175
High Code: 3927
Cycles: 209
Conv Rate: 100.000 kHz
Input Freq: 5.103 kHz
Input Ampl: -0.76 dBFS

Relative: ☐

Harmonic Amplitudes (dBFS)

DC: -56.9
2: -83.0
3: -95.6
4: -92.1
5: -96.3
6: -104.8
7: -98.0
8: -103.3
9: -99.0
10: -105.5
11: -111.6
12: -100.4

Save to File

Working Directory: C:\ATS4000
Full File Name: DUT
Part Information: DUT

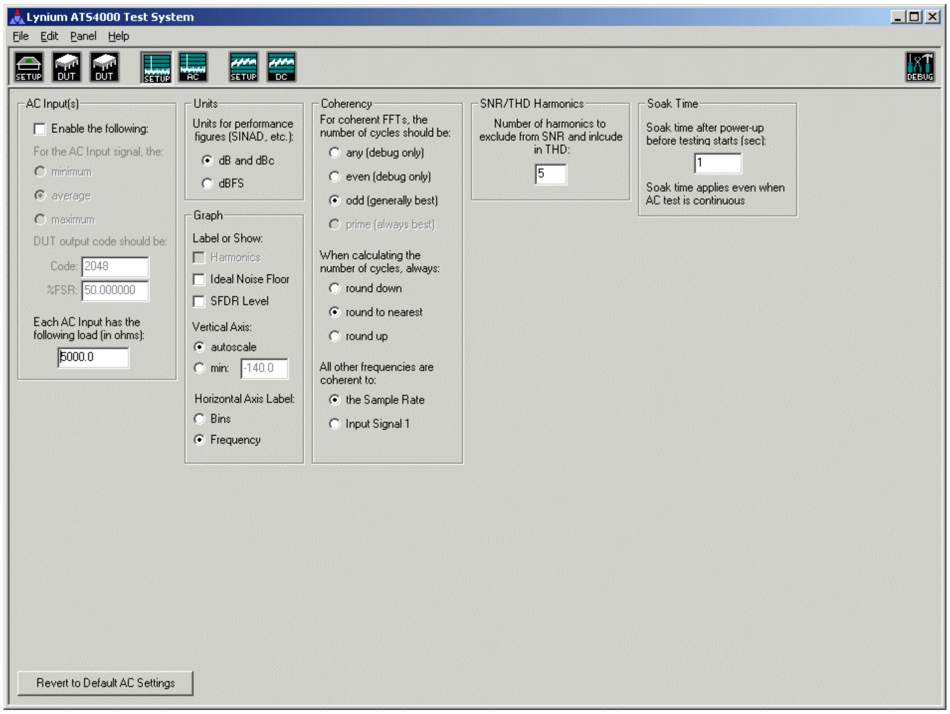
☑ Header
☑ Bin Amplitude
☑ Bin # & Freq.
☐ ADC Results
○ Comma Sep.
● Tab Separated

Information for Most Recent Test Results

11:34:44 2/18/2004 Part: VDD: 5.000138V, 0.365mA, -IN: 0.000087V, VREF: 4.999947V, conv rate: 100000.000Hz, clks per conv: 32. AC Test: continuous, no soak. System #2, test head: GAP1616 #2, daughtercard: ARM6444 #2.

Figure 5. AC Test Result (GAP1616 Test Head installed; 12-bit, 100 kHz ADC).

The AC Test Setup panel is shown in Figure 6. This allows the user to customize the results displayed in the AC Test panel.



AC Input(s)

☐ Enable the following:

For the AC Input signal, the:
○ minimum
● average
○ maximum

DUT output code should be:
Code: 2048
%FSR: 50.000000

Each AC Input has the following load (in ohms): 5000.0

Units

Units for performance figures (SINAD, etc.):
● dB and dBc
○ dBFS

Graph

Label or Show:
☐ Harmonics
☐ Ideal Noise Floor
☐ SFDR Level

Vertical Axis:
● autoscale
○ min: -140.0

Horizontal Axis Label:
○ Bins
● Frequency

Coherency

For coherent FFTs, the number of cycles should be:
○ any (debug only)
○ even (debug only)
● odd (generally best)
○ prime (always best)

When calculating the number of cycles, always:
○ round down
● round to nearest
○ round up

All other frequencies are coherent to:
● the Sample Rate
○ Input Signal 1

SNR/THD Harmonics

Number of harmonics to exclude from SNR and inlcude in THD: 5

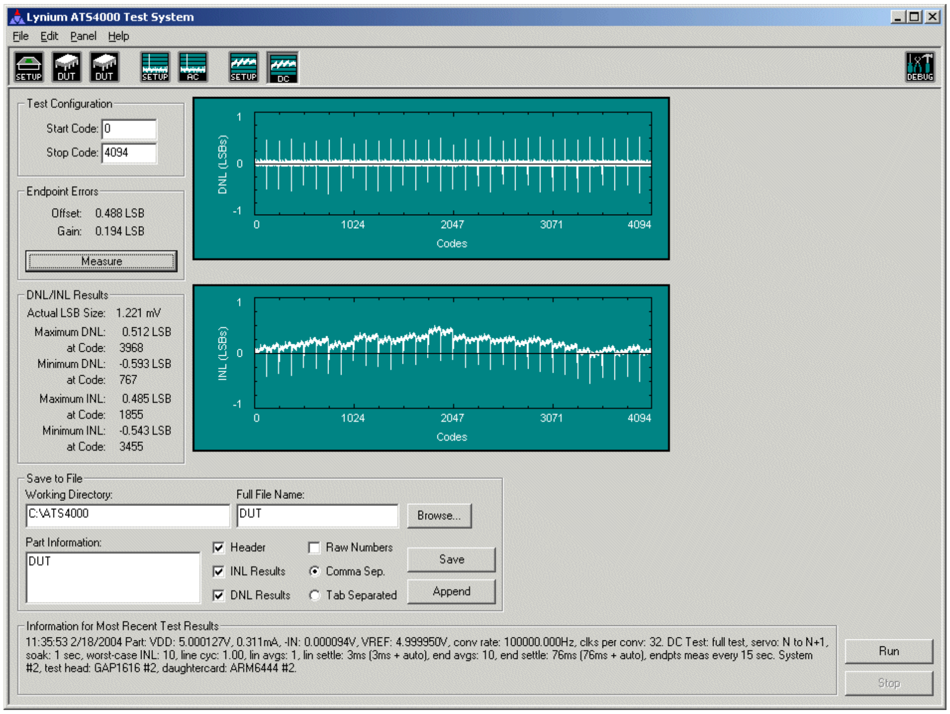
Soak Time

Soak time after power-up before testing starts (sec): 1

Soak time applies even when AC test is continuous

Figure 6. AC Test Setup Panel.

The second of the three tests is the DC linearity test. An example result for a 12-bit, 100 kHz ADC is shown in Figure 7. This test provides offset error, gain error, integral non-linearity (INL) and differential non-linearity (DNL). Additional parameters are provided for help in interpreting the test results.



Test Configuration
Start Code: 0
Stop Code: 4094

Endpoint Errors
Offset: 0.488 LSB
Gain: 0.194 LSB

DNL/INL Results
Actual LSB Size: 1.221 mV
Maximum DNL: 0.512 LSB
at Code: 3968
Minimum DNL: -0.593 LSB
at Code: 767
Maximum INL: 0.485 LSB
at Code: 1855
Minimum INL: -0.543 LSB
at Code: 3455

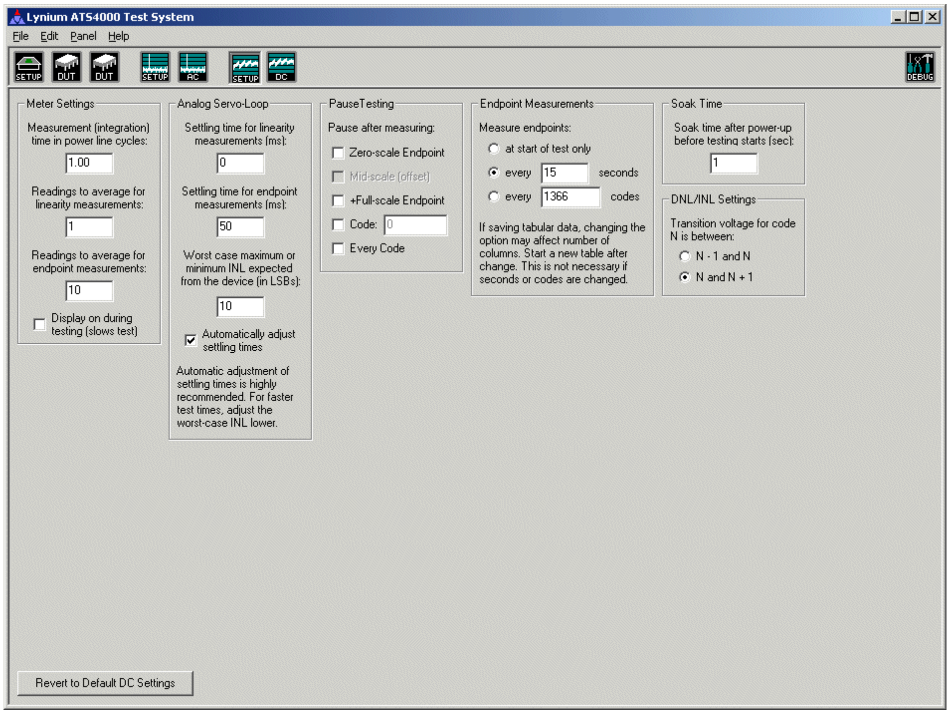
Save to File
Working Directory: C:\ATS4000
Full File Name: DUT
Part Information: DUT
☑ Header
☑ INL Results
☑ DNL Results
☐ Raw Numbers
● Comma Sep.
○ Tab Separated

Information for Most Recent Test Results

11:35:53 2/18/2004 Part: VDD: 5.000127V, 0.311mA, -IN: 0.000094V, VREF: 4.999950V, conv rate: 100000.000Hz, clks per conv: 32. DC Test: full test, servo: N to N+1, soak: 1 sec, worst-case INL: 10, line cyc: 1.00, lin avgs: 1, lin settle: 3ms (3ms + auto), end avgs: 10, end settle: 76ms (76ms + auto), endpts meas every 15 sec. System #2, test head: GAP1616 #2, daughtercard: ARM6444 #2.

Figure 7. DC Test Result (GAP1616 Test Head installed; 12-bit, 100 kHz ADC).

The DC Test Setup panel is shown in Figure 8. This allows the user to customize the results displayed in the DC Test panel.



Meter Settings

Measurement (integration) time in power line cycles: 1.00

Readings to average for linearity measurements: 1

Readings to average for endpoint measurements: 10

☐ Display on during testing (slows test)

Analog Servo-Loop

Settling time for linearity measurements (ms): 0

Settling time for endpoint measurements (ms): 50

Worst case maximum or minimum INL expected from the device (in LSBs): 10

☑ Automatically adjust settling times

Automatic adjustment of settling times is highly recommended. For faster test times, adjust the worst-case INL lower.

PauseTesting

Pause after measuring:

☐ Zero-scale Endpoint

☐ Mid-scale (offset)

☐ +Full-scale Endpoint

☐ Code: 0

☐ Every Code

Endpoint Measurements

Measure endpoints:

○ at start of test only

● every 15 seconds

○ every 1366 codes

If saving tabular data, changing the option may affect number of columns. Start a new table after change. This is not necessary if seconds or codes are changed.

Soak Time

Soak time after power-up before testing starts (sec): 1

DNL/INL Settings

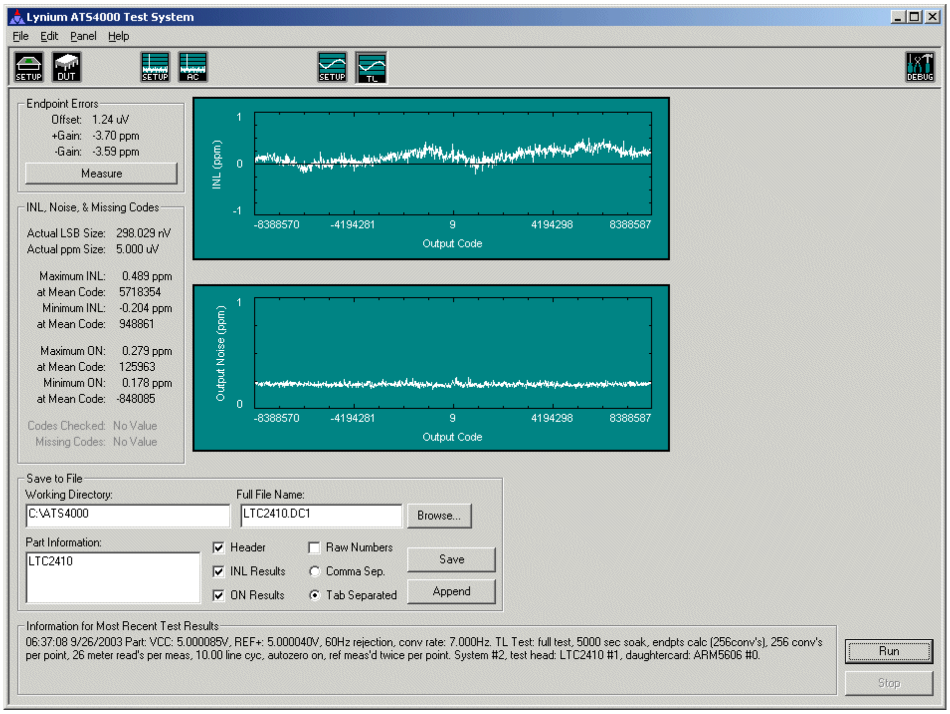
Transition voltage for code N is between:

○ N - 1 and N

● N and N + 1

Figure 8. DC Test Setup Panel.

The third of the three tests is the transfer linearity (TL) test. An example result for a 24-bit, 7.5 Hz ADC is shown in Figure 9. This test provides offset error, gain error, integral non-linearity (INL) and output noise (ON). Additional parameters are provided for help in interpreting the test results.



Endpoint Errors
Offset: 1.24 uV
+Gain: -3.70 ppm
-Gain: -3.59 ppm

INL, Noise, & Missing Codes
Actual LSB Size: 298.029 nV
Actual ppm Size: 5.000 uV

Maximum INL: 0.489 ppm
at Mean Code: 5718354
Minimum INL: -0.204 ppm
at Mean Code: 948861

Maximum ON: 0.279 ppm
at Mean Code: 125963
Minimum ON: 0.178 ppm
at Mean Code: -848085

Codes Checked: No Value
Missing Codes: No Value

Save to File
Working Directory: C:\ATS4000
Full File Name: LTC2410.DC1
Part Information: LTC2410

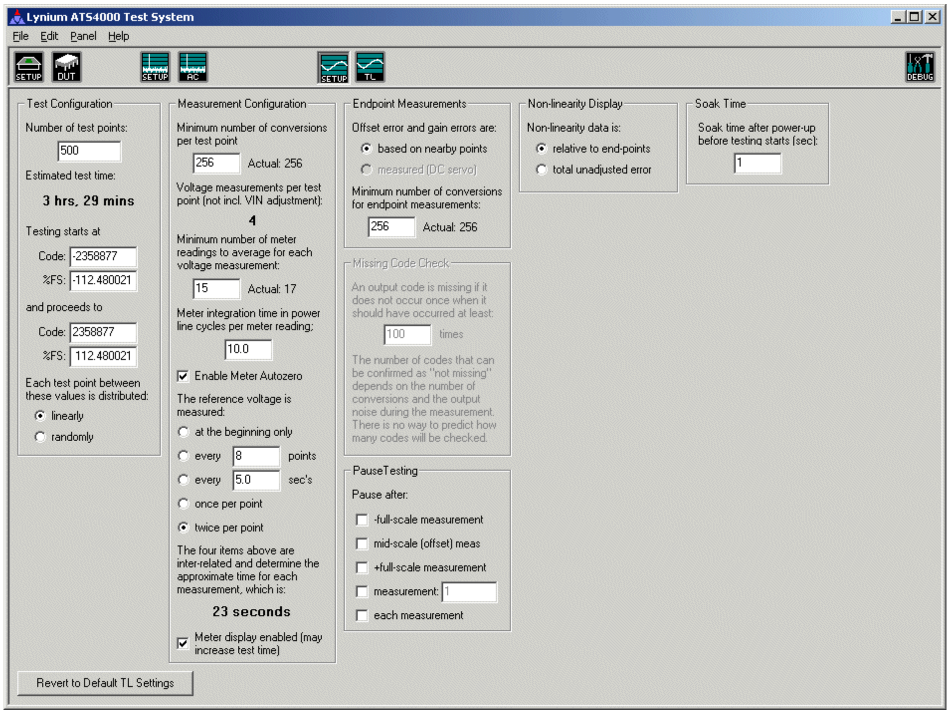
☑ Header
☑ INL Results
☑ ON Results
☐ Raw Numbers
○ Comma Sep.
● Tab Separated

Information for Most Recent Test Results

06:37:08 9/26/2003 Part: VCC: 5.000085V, REF+: 5.000040V, 60Hz rejection, conv rate: 7.000Hz. TL Test: full test, 5000 sec soak, endpts calc (256conv's), 256 conv's per point, 26 meter read's per meas, 10.00 line cyc, autozero on, ref meas'd twice per point. System #2, test head: LTC2410 #1, daughtercard: ARM5606 #0.

Figure 9. TL Test Result (LTC2410 Test Head installed; 24-bit, 7.5 Hz ADC).

The TL Test Setup panel is shown in Figure 10. This allows the user to customize the results displayed in the TL Test panel.



Test Configuration

Number of test points: 500

Estimated test time: **3 hrs, 29 mins**

Testing starts at

Code: -2358877

%FS: -112.480021

and proceeds to

Code: 2358877

%FS: 112.480021

Each test point between these values is distributed:

● linearly

○ randomly

Measurement Configuration

Minimum number of conversions per test point: 256 Actual: 256

Voltage measurements per test point (not incl. VIN adjustment): **4**

Minimum number of meter readings to average for each voltage measurement: 15 Actual: 17

Meter integration time in power line cycles per meter reading; 10.0

☑ Enable Meter Autozero

The reference voltage is measured:

○ at the beginning only

○ every 8 points

○ every 5.0 sec's

○ once per point

● twice per point

The four items above are inter-related and determine the approximate time for each measurement, which is: **23 seconds**

☑ Meter display enabled (may increase test time)

Endpoint Measurements

Offset error and gain errors are:

● based on nearby points

○ measured (DC servo)

Minimum number of conversions for endpoint measurements: 256 Actual: 256

Missing Code Check

An output code is missing if it does not occur once when it should have occurred at least: 100 times

The number of codes that can be confirmed as "not missing" depends on the number of conversions and the output noise during the measurement. There is no way to predict how many codes will be checked.

PauseTesting

Pause after:

☐ -full-scale measurement

☐ mid-scale (offset) meas

☐ +full-scale measurement

☐ measurement: 1

☐ each measurement

Non-linearity Display

Non-linearity data is:

● relative to end-points

○ total unadjusted error

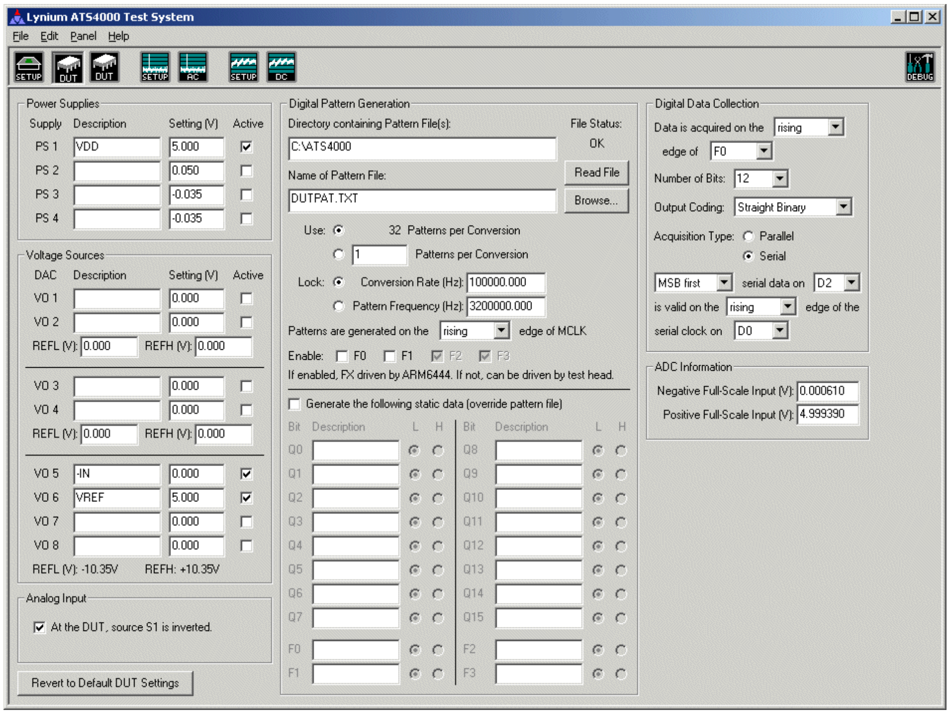
Soak Time

Soak time after power-up before testing starts (sec): 1

Figure 10. TL Test Setup Panel.

For each custom test head, a unique DUT Setup panel is also available. This allows the user to configure the DUT’s power supply (or supplies), reference voltage (or voltages), conversion rate, etc. The exact parameters that can be configured vary depending on the device.

The GAP1616 Test Head is available for customers that wish to test ADCs without relying on Lynium to provide custom test heads and software. More information on the GAP1616 can be found in the GAP1616 Test Head Manual available from the Support section of Lynium’s web site: http://www.lynium.com. The GAP1616 Test Head has two DUT setup panels which are shown in Figures 11 and 12. Rather than provide specific configuration options, the GAP1616 Test Head provides a variety of resources which the user can configure as necessary.



Power Supplies

Supply	Description	Setting (V)	Active
PS 1	VDD	5.000	☑
PS 2		0.050	☐
PS 3		-0.035	☐
PS 4		-0.035	☐

Voltage Sources

DAC	Description	Setting (V)	Active
VO 1		0.000	☐
VO 2		0.000	☐

REFL (V): 0.000 REFH (V): 0.000

DAC	Description	Setting (V)	Active
VO 3		0.000	☐
VO 4		0.000	☐

REFL (V): 0.000 REFH (V): 0.000

DAC	Description	Setting (V)	Active
VO 5	-IN	0.000	☑
VO 6	VREF	5.000	☑
VO 7		0.000	☐
VO 8		0.000	☐

REFL (V): -10.35V REFH: +10.35V

Analog Input

☑ At the DUT, source S1 is inverted.

Revert to Default DUT Settings

Digital Pattern Generation

Directory containing Pattern File(s): C:\ATS4000

File Status: OK

Name of Pattern File: DUTPAT.TXT

Read File

Browse...

Use: ● 32 Patterns per Conversion

○ 1 Patterns per Conversion

Lock: ● Conversion Rate (Hz): 100000.000

○ Pattern Frequency (Hz): 3200000.000

Patterns are generated on the rising edge of MCLK

Enable: ☐ F0 ☐ F1 ☑ F2 ☑ F3

If enabled, FX driven by ARM6444. If not, can be driven by test head.

☐ Generate the following static data (override pattern file)

Bit	Description	L	H	Bit	Description	L	H
Q0		●	○	Q8		●	○
Q1		●	○	Q9		●	○
Q2		●	○	Q10		●	○
Q3		●	○	Q11		●	○
Q4		●	○	Q12		●	○
Q5		●	○	Q13		●	○
Q6		●	○	Q14		●	○
Q7		●	○	Q15		●	○
F0		●	○	F2		●	○
F1		●	○	F3		●	○

Digital Data Collection

Data is acquired on the rising edge of F0

Number of Bits: 12

Output Coding: Straight Binary

Acquisition Type: ○ Parallel ● Serial

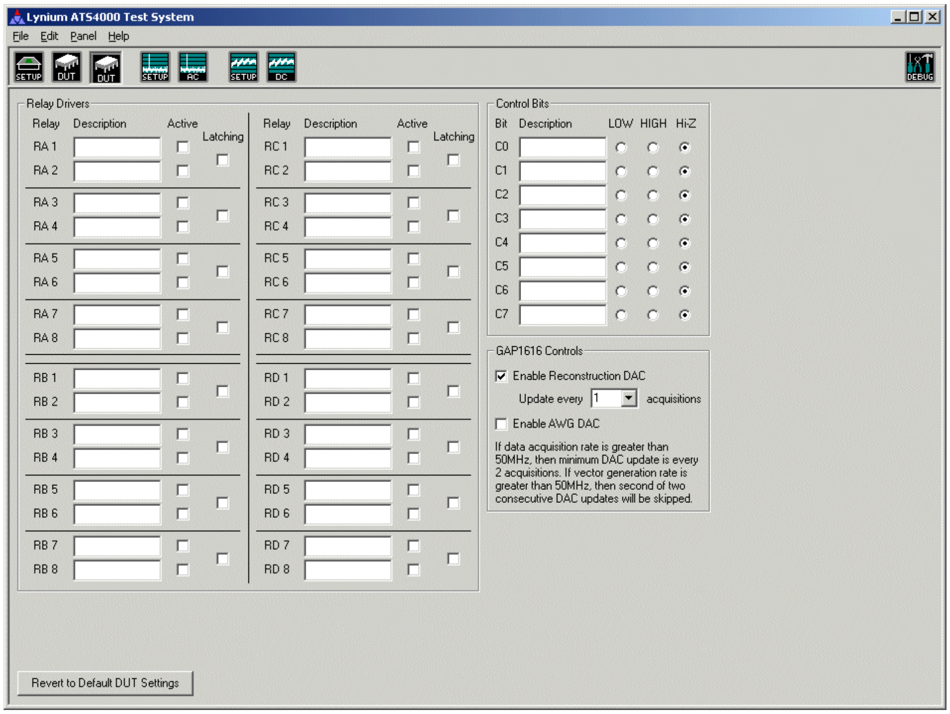
MSB first serial data on D2 is valid on the rising edge of the serial clock on D0

ADC Information

Negative Full-Scale Input (V): 0.000610

Positive Full-Scale Input (V): 4.999390

Figure 11. GAP1616 DUT Configuration Panel #1.



Relay Drivers

Relay	Description	Active	Latching	Relay	Description	Active	Latching
RA 1		☐	☐	RC 1		☐	☐
RA 2		☐		RC 2		☐	
RA 3		☐	☐	RC 3		☐	☐
RA 4		☐		RC 4		☐	
RA 5		☐	☐	RC 5		☐	☐
RA 6		☐		RC 6		☐	
RA 7		☐	☐	RC 7		☐	☐
RA 8		☐		RC 8		☐	
RB 1		☐	☐	RD 1		☐	☐
RB 2		☐		RD 2		☐	
RB 3		☐	☐	RD 3		☐	☐
RB 4		☐		RD 4		☐	
RB 5		☐	☐	RD 5		☐	☐
RB 6		☐		RD 6		☐	
RB 7		☐	☐	RD 7		☐	☐
RB 8		☐		RD 8		☐	

Control Bits

Bit	Description	LOW	HIGH	Hi-Z
C0		○	○	●
C1		○	○	●
C2		○	○	●
C3		○	○	●
C4		○	○	●
C5		○	○	●
C6		○	○	●
C7		○	○	●

GAP1616 Controls

☑ Enable Reconstruction DAC

Update every 1 acquisitions

☐ Enable AWG DAC

If data acquisition rate is greater than 50MHz, then minimum DAC update is every 2 acquisitions. If vector generation rate is greater than 50MHz, then second of two consecutive DAC updates will be skipped.

Revert to Default DUT Settings

Figure 12. GAP1616 DUT Configuration Panel #2.

7. ATS4000 Specifications

Base System

Analog Servo Loop	
Voltage Range	±10.3 V
Voltage Resolution	Infinite
Voltage Noise	5 µVrms (80 kHz Bandwidth)
Current	±25 mA
Digital Servo Loop	
Voltage Range	±10.01 V
Voltage Resolution	3 µV
Voltage Noise	5 µVrms (80 kHz Bandwidth)
Current	±25 mA
Digital I/O	
Number	13 (Base Unit)
Speed	16 MHz I/O data rates
Power Supplies	
Adjustable	
Number	2
Range	+0.035 V to +19.75 V
Voltage Noise	5 µVrms (80 kHz Bandwidth)
Current	100 mA
Adjustable	
Number	2
Range	–19.75 V to –0.035 V
Voltage Noise	5 µVrms (80 kHz Bandwidth)
Current	–100 mA
Fixed, +5 V	
Number	1
Range	5.0 V to 5.3 V
Current	+1 A
Voltage Noise	50 µVrms (80 kHz Bandwidth)
Fixed, –5 V	
Number	1
Range	–5.4 V to –5.1 V
Current	–1 A
Voltage Noise	50 µVrms (80 kHz Bandwidth)
Fixed, +15V	
Number	1
Range	+14.4 V to +15.6 V
Current	+0.5 A
Voltage Noise	50 µVrms (80 kHz Bandwidth)

Fixed, –15V

Number	1
Range	–15.6 V to –14.4 V
Current	–0.5 A
Voltage Noise	50 µVrms (80 kHz Bandwidth)

Mechanical

Dimension	21.5" W X 14.0" D X 6.5" H
Weight	50 Lbs.

ARM6444 Daughtercard

Digital I/O

Number	64
Speed	80 MHz Pattern Generation, 50 MHz Data Capture

Voltage Sources, Adjustable

Number	2
Low Range	–10.25 V to +10.25 V
High Range	Low Range to +10.25 V
Range Resolution	325 µV
Output Resolution	Range / 65,536
Current	±1 mA

Number	2
Low Range	–10.25 V to +10.25 V
High Range	Low Range to +10.25 V
Range Resolution	325 µV
Output Resolution	Range / 65,536
Current	±1 mA

Voltage Sources, Fixed

Number	4
Range	–10.25 V to +10.25 V
Resolution	325 µV
Current	±1 mA

ARM5606 Daughtercard

Voltage Sources

Number	3 Differential to 6 Single-ended
Range (single-ended)	–10.01 V to +10.01 V
Resolution (single-ended)	305 nV (76 nV in some modes)
Current (single-ended)	±1 mA
Voltage Noise (single-ended)	6 µVpp (0.1 Hz to 10 Hz bandwidth)
Frequency Range	0.001 Hz to 10 kHz
Frequency Resolution	2 pHz

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8. Version History

Ver.	Date	Comment
--	April 11, 2000	Draft Release
A	June 1, 2001	Added pictures and specifications
B	October 15, 2001	Added software “screen shots.”
C	February 11, 2004	Re-formatted and updated to reflect recent ATS4000 developments.