ATS4000 Advanced Test System

# Offset Error & Gain Error Correlation Issues
with the ATS4000

*Version*: B

**Lynium**

May 18, 2000
Tucson, Arizona

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Document:
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Version B
May 18, 2000
Lynium Document Number: ATS4K04B

Comments, corrections, and suggestions regarding this document are always welcomed by the author.

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Abstract

This document discusses offset error and gain error correlation issues that might arise between the ATS4000 and other test systems, particularly production test equipment. There are a variety of mechanisms which can produce discrepancies between two different test systems, but there are several common sources of error when testing analog-to-digital converters. These error sources are described in this document and several “questions and answers” presented regarding correlation issues.

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## 1. Typical Offset Error and Gain Error Correlation Problems

All test systems have two primary goals: precision and accuracy. Accuracy always equates to precision, but the reverse is not true. Accuracy is defined as achieving the correct result (relative to a given standard) while precision implies achieving the same result from test to test. Inherent in both accuracy and precision is an assumption that the result is repeatable to a desired level.

Thus, if the answer is correct, then it is also precise. However, the answer can be precise without being correct (accurate).

In regards to a test system, precision is related to repeatability while accuracy is related to both repeatability and correlation. In general, the production environment is concerned with repeatability (producing products which are identical to each other). However, accuracy becomes a concern when comparing results produced by two different systems. It is always easier to achieve precision than to achieve accuracy, so correlation is more difficult than repeatability.

For an analog-to-digital converter (ADC), two of the hardest measurements to correlate are offset error and gain error. These are difficult because both are directly related to making accurate measurements of voltage levels. In comparison, integral non-linearity (INL) and differential non-linearity (DNL) are not nearly as difficult. These measurements are made relative to the offset error and gain error. Thus, changes in gain error and offset error tend to have little impact on INL and DNL (the transfer function shifts, but does not change its overall shape).

An example of a gain error correlation issue can be seen by comparing Figures 1 and 2. The two "DC" test results (offset error, gain error, INL, and DNL) are for the same 12-bit, 100kHz ADC. However, a difference can be seen in the gain error results: –0.5LSB vs. –0.1LSB. The only difference between the two tests is the impedance of the source driving the analog input of the converter.

Note that the results for the other DC measurements show good precision:

| | Offset Error (LSB) | Gain Error (LSB) | Max. DNL (LSB) | Min. DNL (LSB) | Max. INL (LSB) | Min. INL (LSB) |
|---|---|---|---|---|---|---|
| Figure 1 Results | 1.12 | -0.51 | 0.31 | -0.18 | 0.63 | -0.12 |
| Figure 2 Results | 1.18 | -0.09 | 0.32 | -0.23 | 0.63 | -0.12 |

Table I. Comparison of Results from Figures 1 and 2.

The difference in offset error and minimum DNL is the only significant differences between the two sets of results. These have changed 0.06LSB and 0.05LSB, respectively. However, this degree of change is very slight and would not generally present a correlation issue.

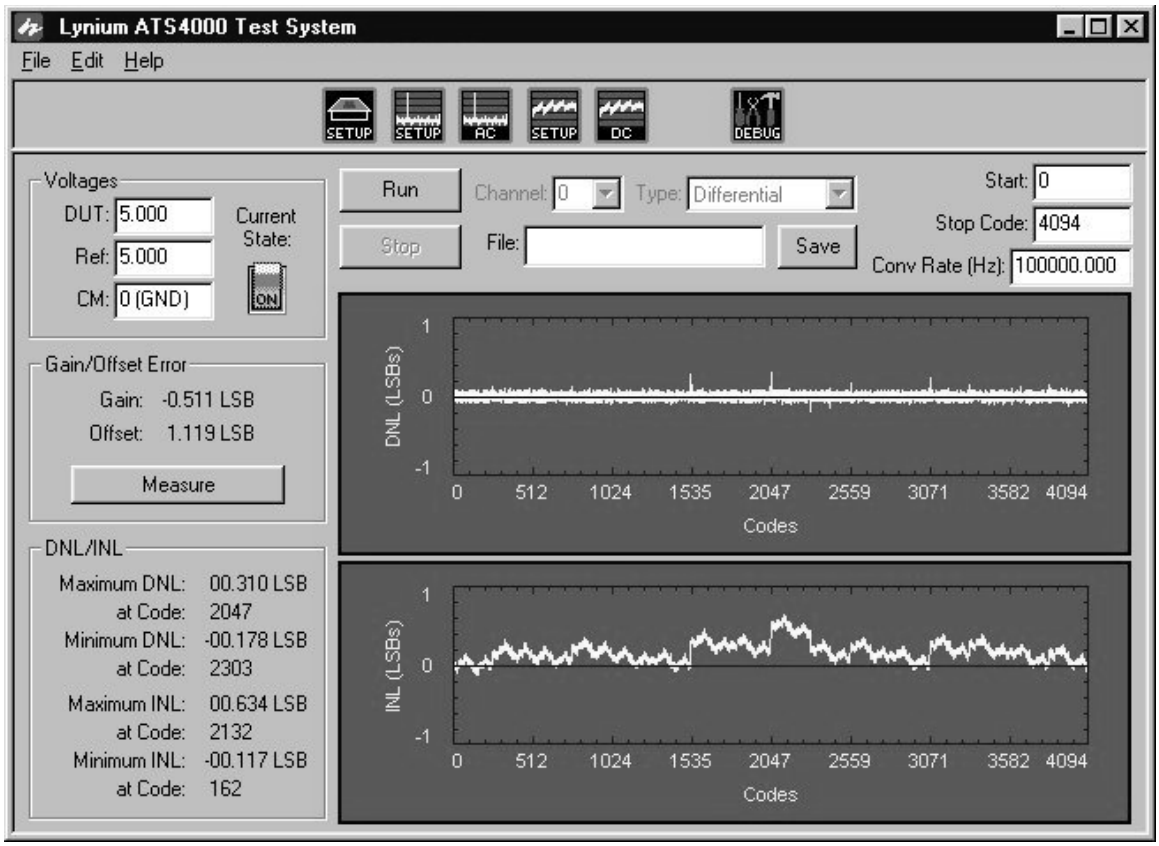

Figure 1. “DC” Measurements on a 12-bit, 100kHz ADC.

 

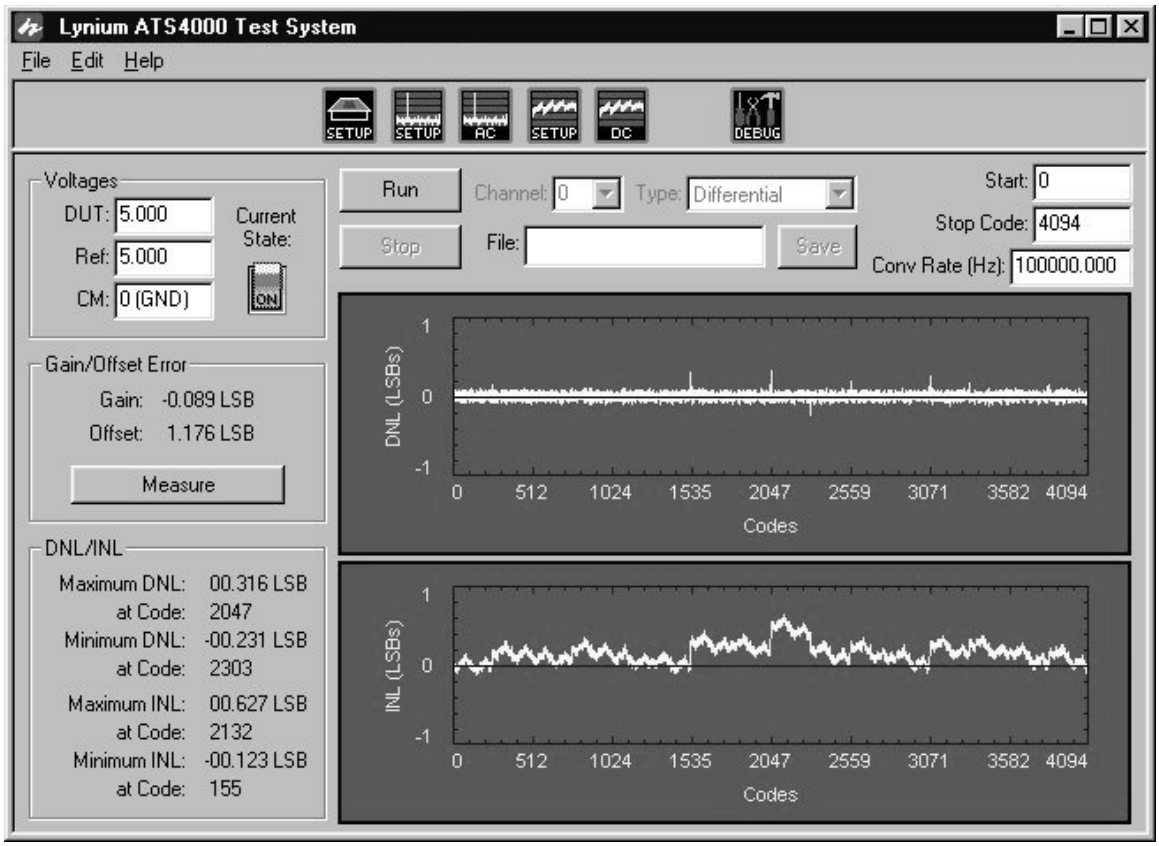

Figure 2. Same ADC as Figure 1 with a Different Input Configuration.

## 2. Sources of Offset Error and Gain Error Shifts

With ADCs, there are four common reasons why the voltage measurements associated with DC tests are not accurate: change in impedance of the ground pin or pins between different layouts, change in impedance of the source driving the converter's input, change in impedance of the source driving the converter's reference, and charge injection at the sample-and-hold.

Ideally, the DC results are obtained in such a way that nothing changes at the pins of the ADC being tested. Unfortunately, the analog input voltage must change in order to accomplish the test. The change in the analog input voltage can produce a change in the charge injection seen at the sample-and-hold as well as the loading seen at the reference. In addition, the current in the ground pin or pins of the ADC will also change.

Taking the ground current first, any change in the impedance of the ground pin or pins will change the "ground" reference point of the integrated circuit. Thus, offset can change from one test board to the next, particularly if one test board is an engineering evaluation board with a low-profile socket and the other a production test board with a socket designed for use with a handler. Everything being equal, ADCs with lower power will have fewer problems in measuring offset error accurately. For higher power ADCs, care

must be taken in lowering the impedance of all ground connections, including the layout of the test board.

The impedance of the circuitry driving both the analog input and the reference input (if present) must also be lowered. However, there are two different ways to do this: placing a large capacitor with low equivalent series resistance (ESR) right at the pin or by using a very fast settling circuit such as a high-speed amplifier. In the later case, the capacitance at the pin must be reduced in order to ensure that the circuit settles quickly. So, these two approaches are diametrically opposed.

For the reference input, placing a large capacitor (1µF to 10µF in parallel with a 0.1µF) at the reference input is usually the preferred choice. In the ADCs datasheet, a capacitor that is similar in size to that used on the production test board can be recommended. This helps the customer achieve ADC performance that matches the datasheet specifications.

The analog input is a different matter altogether. If a large capacitor is used at the analog input, then test times can suffer while the analog input settles to the appropriate level. On the other hand, using a high-speed amplifier to drive the converter possess a problem with the datasheet. Good high-speed amplifiers can greatly exceed the cost of the converter, making it impractical to recommend in the datasheet. Thus, end-users of the ADC may have difficulty getting "specified" performance from the ADC.

The problem here is really an issue of measuring the voltage at the converter's input. The ADC does not see the analog input continuously, but is always taking a 'snapshot" of the analog input. This snapshot, taken by the sample-and-hold, changes the input voltage. Unfortunately, the device that measures the input voltage is usually an integrating voltmeter, and it continuously measures the voltage over a given period of time.

Figure 3 shows the input voltage to an ADC. At the start of the acquisition time ($t_{ACQ}$), the input voltage is "glitched" as the sample-and-hold goes into the sample mode. There are two reasons for this: charge injection coming out of the sample-and-hold and the sudden appearance of a small capacitive load at the converter's input (usually 20pF or so). Unless the source impedance is very low (such as a very large capacitance with low ESR), the input voltage will change slightly.

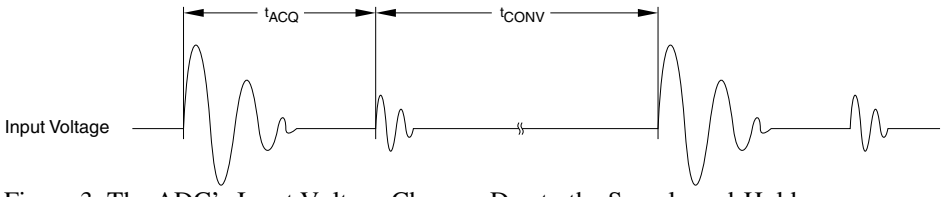

Figure 3. The ADC's Input Voltage Changes Due to the Sample-and-Hold.

The ADC only "senses" the voltage at its input which is present just before the sample-and-hold goes into the hold mode. Thus, the voltage which is present at the end of $t_{ACQ}$ is the voltage that is acquired by the ADC. However, the voltmeter measuring the input

 

voltage measures the entire waveform. These two voltages may differ from one another by a few hundred microvolts or more.

As a brief side note, if the ADC is an integrating converter, then the measurement at the voltmeter should correlate much more closely to the input voltage at the ADC's input (another help is that integrating converters do not have sample-and-holds). On the other hand, a very high-speed converter (a few megahertz and beyond) can produce so much "noise" on the analog input, that the voltage seen by the voltmeter may be several millivolts different from the voltage seen by the converter. This is why direct DC measurements are typically not performed on high-speed ADCs.

A problem related to the glitching of the analog input is charge injection. The sample-and-hold of most modern ADCs is simply a switch followed by a small capacitor as shown in Figure 4. The sample-and-hold signal which is produced within the ADC controls the state of the switch.

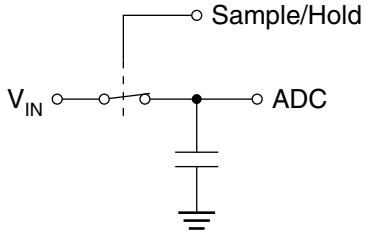

Figure 4. Ideal Sample-and-Hold Circuit.

Figure 5 shows an actual sample-and-hold as implemented on a CMOS ADC. When the sample-and-hold signal transitions from high-to-low or vice-versa, charge is driven off the gate (or onto the gate, as the case may be), into the driving circuitry, and also onto the sampling capacitor. This results in glitching of the source driving the input voltage and an increased (or reduced) voltage on the sampling capacitor.

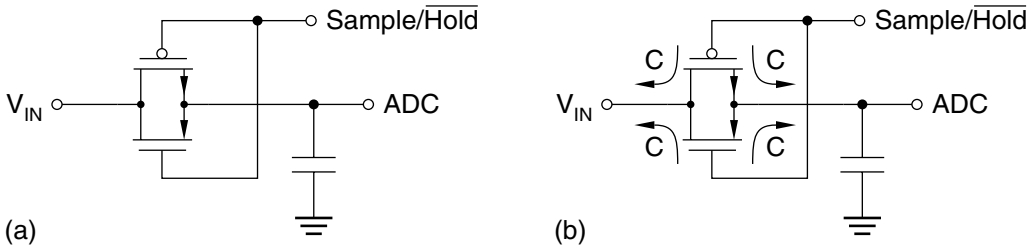

Figure 5. (a) Actual Sample-and-Hold Circuit and (b) with Charge Injection Shown During a Transition of the Sample/*Hold Signal.

Amazingly, the charge injection voltage shift produced by the sample-and-hold switch is generally constant over the ADCs transfer range. This means that the percentage of charge which goes out of the ADC compared to the percentage that ends up on the sampling capacitor remains constant. However, from one test configuration to the next, the percentage is likely to change. That change can result in changes to both offset error and gain error.

## 3. Common Questions Regarding Correlation Issues

*"What's the best way to achieve correlation?"*

The single best way to achieve as much correlation as possible is to make sure that all test configurations drive the ADC in the same way and use the same measurement equipment. This means using the same circuit configuration, the same op-amps, similar layouts, similar sockets, and the exact same voltmeter.

*"Isn't that sweeping the problem under the rug?"*

In some regards, that is certainly true. However, semiconductor companies have been fighting this problem for many years and have not come up with an effective, general-purpose solution. Manufacturing is usually concerned with making sure that delivered product falls within some acceptable range of variability. The end-user is also concerned with repeatability from part-to-part, not accuracy to a known standard—provided that the accuracy is "reasonable." However, the importance of repeatability and accuracy to the end-user must be assessed for each product. Also, it is important that the test configuration be shown in the product's datasheet or available to customers should they request the information. Access to the exact production configuration allows the customer some control in matching ADC performance in their system to the ADC's specifications.

*"But isn't it impossible to use the same test system in all cases?"*

There are two broad reasons to measure an ADCs performance: for engineering evaluation and characterization, and for production test. It is difficult to serve these two masters with one common test platform. However, it is still possible to minimize the differences. For example, using the same type of op-amp to drive the converter's analog input, always using the same value and type of capacitor for bypassing the reference, using a common printed-circuit board (PCB) layout, etc. Keep in mind that even with the exact same PCB in similar production equipment, it will be difficult to achieve correlation of offset error and gain error. This is particularly true of converters with resolutions of 16-bits or more. A reasonable method of addressing the discrepancies must also be developed.

*"What's the typical correlation error?"*

It is difficult to provide a "typical" figure as it changes from test system to test system and with the type of device being measured. Measurement of the voltage at the input of an ADC is generally accurate to about one millivolt for an "industrial" successive approximation register (SAR) ADC. This value mostly depends on the ADC and driving circuitry and is only somewhat dependent on the test system. On the other hand, repeatability typically depends on the care taken in the overall test system. For example, one-sigma repeatability of the ATS4000 is typically below 10µV (the ATS4000 software allows the user to trade-off repeatability for test time).

 

*"In Figures 1 and 2, the DNL and INL doesn't change even though gain error changes. Why is that and will that always be the case?"*

No, there is no guarantee that DNL and INL will always correlate even thought offset error and gain error may not correlate. It's possible that socketing issues, layout differences, and charge injection problems may produce differences in INL and DNL between two test configurations. However, in general, it seems that INL and DNL seem to have similar "signatures" even thought offset error and gain error may differ by one or more LSBs.

*"What you're really talking about is gain error and offset error versus source impedance. Isn't that true?"*

Yes, that is the main issue here. Gain error and offset error can be graphed as a function of the impedance of the source driving the converter. Usually, both errors will change very little as source impedance is increased from "zero" until the performance reaches a knee and the errors begin to increase dramatically. However, as what was mentioned in this document, the main problem is the impedance of the driving source during the sampling period, which can be a relatively short period of time. This period can roughly be equated to a frequency by taking its reciprocal, but this is only a first-order approximation as other factors can come into play. So, what's really needed in order to assess this problem in an engineering manner is to know the gain error and offset error of the ADC versus source impedance, the impedance of each possible source over frequency, and the equivalent "frequency" of the sampling period (as seen by the component driving the converter).

While a typical "Gain Error and Offset Error vs. Source Impedance" graph can be a very useful item to include in the product's datasheet, this graph is not done very often. When it is done, it is often based on a small number of parts and/or widely spaced data points. The goal is generally to find the knee where the source impedance becomes a problem, not to find small changes in gain error or offset error (on the order of what is being discussed here) versus small changes in input impedance. Knowing what data is needed does not necessarily make the problem any easier.

## Revision History

| Rev. | Date | Comment |
|---|---|---|
| A | April 4, 2000 | Initial Release |
| B | May 18, 2000 | Revised figures 1 and 2 and added “source impedance” question |

 